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the buffer structure having a height larger than a width thereof so as to suppress a stress applied to the capacitor dielectric film caused by a thermal expansion coefficient difference between the substrate and the capacitor dielectric film.

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3. (Amended) A capacitor comprising:

a lower electrode formed on a substrate

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a capacitor dielectric film formed on the lower electrode, and formed of a perovskite ferroelectric material having a larger thermal expansion coefficient than that of the substrate and having a crystal oriented substantially perpendicular to a surface of the lower electrode; and

an upper electrode formed on the capacitor dielectric film,

the lower electrode having a height larger than a width thereof so as to suppress a stress applied to the capacitor dielectric film caused by a thermal expansion coefficient difference between the substrate and the capacitor dielectric film.

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14. (Amended) A semiconductor device comprising:

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a memory cell transistor formed on a semiconductor substrate and including a gate electrode, and source/drain diffused layers formed in the semiconductor substrate respectively on both sides of the gate electrode;

an insulation film covering the semiconductor substrate with the memory cell transistor formed on; and

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a capacitor formed on the insulation film, and including a lower electrode electrically connected to one of the source/drain diffused layers; a capacitor dielectric film formed on the lower electrode, and formed of a perovskite ferroelectric material having a larger thermal expansion coefficient than that of the semiconductor substrate and having a crystal oriented substantially perpendicular to a surface of the lower electrode; and an upper electrode formed on the capacitor dielectric film,

the lower electrode having a height larger than a width thereof so as to suppress a stress applied to the capacitor dielectric film caused by a thermal expansion coefficient difference between the substrate and the capacitor dielectric film.

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